Final report for CENIIT project 03.03 (2003-08)

Testability-Oriented Design Techniques for Mixed-Signal/RF Integrated Circuits

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In this project we have developed design techniques which facilitate test for mixed-signal/RF integrated circuits. We have focused on systems including RF transceivers. A system with both transmitter, receiver and the accompanying digital part have been used as a platform for our study of testability. In such a case the analog RF front-end can be reconfigured for test while the available baseband processor can serve as a tester. Loopback and bypassing are the enabling on-chip techniques supported by embedded observation blocks. By using this approach the fault-oriented *go*/*no-go* test and also some specification-oriented RF tests can be carried out. Both the RF test methods and design for test (DfT) techniques have been addressed in this project. CMOS technology was exploited to verify the DfT concepts in practice.

1 Scientific results

Since 2003 the project evolved from fault modeling for RF CMOS chips through simulation of various test circuitry, test setups, and generation of optimum stimuli to finally reach a stage of practical implementation. Using the developed DfT techniques two RF CMOS chips have been designed, manufactured and successfully measured demonstrating feasibility of the on-chip test with no tradeoff in chip performance. The test technique of a complete transceiver makes use of the loopback setup with bypassing. For best detectability the sensitization techniques have been developed. The limited test observability of some faults can be largely improved by RF detectors which act as noninvasive observation blocks. On-chip calibration technique has been proposed for them. Also the problem of production tolerances typical of analog/RF circuits have been captured in terms of detectability thresholds. Among various measurement problems the wideband impedance matching on a PCB board was successfully solved in this project as well.

The main results obtained comprise the following:

- Loopback BiST model for digital transceivers with limited test circuitry
- Feasibility of loopback BiST for different transceiver architectures
- Loopback test for RF transceivers with direct modulation
- Spot-defects models (typical of CMOS technology) based on noise and nonlinear analysis, using fault abstraction
- Techniques for sensitizing the RF test path for common faults
- Production tolerances and fault masking effect, detectability thresholds
- Mixed test for enhanced fault coverage (SER/EVM, IP3, gain)
- Fast BER/SER test technique for digital transceivers
- Design of test blocks for integration in CMOS technology
- Design of RF receiver front-end for enhanced test controllability

- On-chip RF test bus for enhanced observability
- On-chip calibration of RF detectors
- Design of on-chip two-tone generator for IP3 test
- PCB board design for wideband RF test

The addressed issues cover both the system- and circuit-level test perspective for RF integrated circuits. The results obtained are unique and we believe they pave a way for new test practices to be introduced by industry.

2 Degrees

- Rashad Ramzan, *Flexible Wireless Receivers: On-Chip Testing Techniques and Design for* Test, Lic. Thesis, LiU No. 1378, 2008
- Rashad Ramzan, PhD Thesis defense planned June 2009

3 MS Thesis projects:

1. L. Li, *RF Transceiver Front-End Design for Testability,* Report No. LiTH-ISY-EX-3525-2004, Linkoping 2004, 41 pp.
2. J. Gonzalez Bayon, *Defect Oriented BiST Model for Integrated Circuits RF Transceivers,* Report No. LiTH-ISY-EX-3544-2004, Linkoping 2004, 63 pp.
3. T. Kantasuwan, *RF Front-end CMOS Design for BiST, ,* Report No. LiTH-ISY-EX-3622-2004, Linkoping 2004, 64 pp.
4. X. Sheng, *RF Mixer design for Zero-IF Wi-Fi Receiver in CMOS,* Report No. LiTH-ISY-EX-3614-2005, Linkoping 2005, 63 pp.
5. N. Hai, *UWB Alternative Light RF System Test,* April 2006, (patent pending at Philips) to be published at LiU
6. M. Wasim, *CMOS LNA for Multistandard Applications,* Sept. 2006, Report No. LiTH-ISY-EX-06/3813-SE, Linköping 2006, 60 pp.
7. G. Mehdi, *Highly Linear Mixer for on-Chip RF Test in 130nm CMOS,*, Report No. LiTH-ISY-EX-06/3913-SE, Linköping 2007, 82 pp.

4 Persons supported by the CENIIT grant

The following researchers were partly supported by the grant:

- Jerzy Dąbrowski (project leader)
- Rashad Ramzan (PhD student)
- Shakeel Ahmad (PhD student)

5 Cooperation with industry and relation to other projects

Our research has drawn attention of the test people working in the field. Especially, high costs of production test for RF chips, so far relying on expensive test equipment, have evoked interest at industry for alternative test methods. As a result we gave 2 invited talks at Philips and one at Texas Instruments as reported beneath.
In 2004 we established a link with Philips Research, Eindhoven, NL (contact person Dr Jose Pineda de Gyvez) and formulated a joint project on test for wideband transceivers, completed as MS project during 6 month internship 2005/06 in Eindhoven.
In September 2005 we established a link with Philips Semiconductors (since 2007 NXP), Caen, France, as well. The group supervised by Dr. Patrice Gamand has been interested in

collaboration to implement RF BiST in their demonstration chips. The NDA between LiTH and Philips Semiconductors was signed and a collaboration plan was formulated. During spring 2006 a project work driven by the Philips needs was performed and completed in May 2006. In 2007 we were also consulting NXP's RF chip design aimed at on-chip test and calibration.
During 2007 and 2008 J. Dąbrowski delivered lectures on RF test techniques within a program "Executive Master in Microelectronics" at ENSICAEN/NXP, (Caen, France).

In cooperation with Dr. Erik Larsson (project leader of CENIIT 05.06), J. Dąbrowski and Prof. A. Alvandpour gave a PhD course "Digital/Analog/RF VLSI testing" in May-June 2007. 16 students from different groups attended the course.

During 2006-08 much of the design work within this project was done jointly with the VR project entitled "Direct RF Sampling for Flexible Radio Architectures" led by Prof. C. Svensson (LiTH). Two RF chips provided with DfT features have been designed and verified on bench.

6 Creation of new research group

With the help of the CENIIT grant I could establish a research group oriented at Mixed-Signal/RF IC Design and Design for Testability with currently 2 PhD students and 2 MS students. The research work continues based on VR and SSF funds granted recently.

7 List of publications

1. J. Dabrowski, *BiST Model for IC RF-Transceiver Front-End*, Proc. of Intl. Symposium on Defect & Fault Tolerance in VLSI Systems, (DFT'03), Cambridge, MA, USA, Nov. 2003, 8 pp.
2. J. Dabrowski, *Loopback BiST for RF Front-Ends in Digital Transceivers*, Proc. of Intl. Symposium System-on-Chip, (SoC'03), Tampere, Finland, Nov. 2003, 4 pp.
3. J. Dabrowski, L. Li, *Signal Path Sensitization for Built-in-Self-Test in Integrated RF Transceivers*, Proc of IEEE Design & Diagnostics of Electronic Circuits & Systems Workshop, (DDECS'04), Tatr.Lomnica, Slovakia, April 2004, 8 pp.
4. J. Dabrowski, *Fault Modeling in RF Blocks Based on Noise Analysis*, Proc of IEEE Intl. Symposium on Circuits & Systems (ISCAS'04), Vancouver, Canada, May 2004, 4 pp.
5. J. Dabrowski, J. Gonzalez Bayon, *Mixed Loopback BiST for RF Digital Transceivers,* Proc of Intl. Symposium on Defect & Fault Tolerance in VLSI Systems, (DFT'04), Cannes, France, Oct. 2004, 8 pp.
6. J. Dabrowski, J. Gonzalez Bayon, *Techniques for Sensitizing RF Path under SER Test,* , Proc of IEEE Intl. Symposium on Circuits & Systems (ISCAS'05), Kobe, Japan, May 23-26, 4 pp.
7. T. Kantasuwan., R.Ramzan, J.Dabrowski, *Programmable RF Attenuator for On-Chip Loopback Test*, Proc. of IEEE European Test Symposium 2005, Tallinn, Estonia, May 2005, 6 pp.
8. T. Kantasuwan., R.Ramzan, J.Dabrowski, *Programmable Attenuator and Switch for RF Test by Chip Reconfguration*, Proc.of RVK'05 Conf., Linköping, Sweden, June 2005, 4 pp.
9. R. Ramzan, J. Dabrowski, *CMOS Blocks for on-Chip RF Test*, Proc.of MIXDES Conf. 2005, Krakow, Poland, June, 2005, 6 pp.
10. R. Ramzan, L. Zou, J. Dabrowski, *LNA Design for on-Chip RF Test,* Proc. of IEEE Intl. Symposium on Circuits & Systems (ISCAS'06), Island of Kos, Greece, May 2006, 4pp.
11. J. Dabrowski, R. Ramzan, *Offset Loopback Test fo IC RF Transceivers,* Proc.of MIXDES Conf., Gdynia, Poland, June 2006, (4 pp)
12. R. Ramzan, J. Dabrowski, *CMOS Blocks for on-Chip RF Test*, Int. J. Analog Integrated Circuits and Signal Processing, Kluwer-Springer, 2006, Vol.49, pp. 151-160

13. J. Dabrowski, *RF on-Chip Test by Reconfiguration Technique,* (*invited*) Proc. of WSEAS Conf. on Circuit & Systems, Athens, Greece, July 2006, 6 pp.
14. J. Dabrowski, R. Ramzan, *Loopback Test for Polar Loop TRx,* report for Philips Semiconductor (F) under NDA, May 2006, 8 pp
15. R. Ramzan, J. Dabrowski, *CMOS RF/DC Voltage Detector for on-Chip Test,* Proc.of INMIC'06, Islamabad, Pakistan, December 2006, pp. 472-476
16. J. Dabrowski, *DfT and BiST Techniques for RF Integrated Circuits*, ENSICAEN/ NXP, Caen, F, 3 April 2007, (distributed lecture notes)
17. J. Dabrowski, R. Ramzan, *Boosting SER Test for RF Transceivers by Simple DSP Technique*, Proc.of DATE Conf., Nice, France, April 2007 (6 pp.)
18. S. Andersson, R. Ramzan, J. Dabrowski, C. Svensson, *Multiband Direct RF Sampling ReceiverFront-End for WLAN in 0.13um CMOS,* Proc. of ECCTD, Seville, Spain, August 2007, pp.168-171
19. R. Ramzan and J. Dabrowski, *On-chip Calibration of RF Detectors by DC Stimuli and Neural Network Technique*, Proc. of IEEE Radio Frequency Integrated Circuits Symposium(RFIC), Atlanta Georgia, USA, June 2008, 4 pp.
20. J. Dabrowski, R. Ramzan, *Built-in Loopback Test for IC RF Transceivers,* under review in IEEE Trans. on VLSI Circuits, (14 pp.)
21. S. Ahmad and J. Dabrowski, *ADC on-Chip Dynamic Test by PWM Technique*, Proc. of ICSES, September 2008, Krakow, Poland, pp 15-18.
22. R. Ramzan, S. Andersson, J. Dabrowski, C. Svensson, *Multiband RF-Sampling Receiver Front-End with On-Chip Testability in 0.13um CMOS*, accepted to Int. J. Analog Integrated Circuits and Signal Processing, Kluwer-Springer, 2009
23. R. Ramzan, J. Fritzin, J. Dabrowski, C. Svensson, *Wideband Low Reflection Transmission Lines for Bare Chip on Multilayer PCB*, under review in IEEE Trans. on Advanced Packaging, (6 pp.)

8 Invited talks and lectures

1. J. Dabrowski, *Defect-Oriented Test for RF Chips – Opportunities and Drawbacks*, Philips Research, Eindhoven, The Netherlands, 26 Nov. 2004
2. J. Dabrowski, *DfT Techniques for RF Transceivers*, Philips Semiconductors, Caen, France, 8 Sept. 2005
3. J. Dabrowski, *RF IC Front-end Design for Testability*, IBCAST Conf., Islamabad, Pakistan, 8-11 Jan. 2007
4. R. Ramzan, *RF Circuit Design for On-Chip Test*, Texas Instruments, Dallas, USA, Feb.2007.
5. J. Dabrowski, *DfT and BiST Techniques for RF Integrated Circuits*, ENSICAEN/ NXP, Caen, France (*invited lectures*) 3 April 2007, 14 Nov 2007, 9 Dec 2008

Related publications:

1. D. Jakonis, K. Folkesson, J. Dabrowski, C. Svensson, *Downconversion Sampling Mixer for Wideband Low-IF RF Receiver*, Proc. of MIXDES'03, Lodz, Poland, June 2003, 6 pp.
2. D. Jakonis, J. Dabrowski, C. Svensson, *Noise Analysis of Downconversion Sampling Mixer*, Proc. of European Conference on Circuit Theory and Design (ECCTD), Cracow, Poland, Sept. 2003, 4 pp.
3. K. Folkesson, D. Jakonis, J. Dabrowski, C. Svensson, *Design of RF Sampling Receiver Front-End,* Proc. of MIXDES'04, Szczecin, Poland, June 2004, 6 pp.

4. D. Jakonis, K. Folkesson, C. Svensson, J. Dabrowski, and P. Eriksson, *An RF Sampling Downconversion Filter for a Receiver Front-End,* Proc. of IEEE Midwest Symposium on Circuits & Systems, (MWSCAS'04), Hiroshima, Japan, July 2004, 4 pp.
5. D. Jakonis, K. Folkesson, J. Dabrowski, P. Eriksson, C. Svensson: *A 2.4-GHz RF sampling receiver front-end in 0.18µm CMOS*, IEEE J. of Solid-State Circuits, Vol. 40, Issue 6, June 2005, pp 1265 - 1277
6. S. Andersson, J. Konopacki, J. Dabrowski, C. Svensson, *RF Sampling Mixer for Zero-IF Receiver with High Image-Rejection*, Proc. of MIXDES Conf. 2005, Krakow, Poland, June 2005, 4 pp.
7. S. Andersson, J. Konopacki, J. Dabrowski, C. Svensson, *RF Sampling Mixer for Zero-IF Receiver with High Image-Rejection*, Int. J. Analog Integrated Circuits and Signal Processing, Kluwer-Springer, 2006, Vol.49, pp. 115-122
8. S. Andersson, J. Konopacki, J. Dabrowski, C. Svensson, *Noise Analysis and Noise Estimation of an RF Sampling Front-end Using SC Decimation Filter, ,* Proc.of MIXDES Conf. 2006, Gdynia, Poland, 22-24 June, 2006, 6 pp.
9. J. Dabrowski, S. Andersson, C. Svensson, , J. Konopacki, *SC Filter Design for RF Applications,* Proc. of ICSES, Lodz, Poland, Sept. 2006, 4 pp.
10. R. Ramzan, S. Andersson, J. Dabrowski, C. Svensson, *A* 1.4V*,* 25mW *Inductorless Wideband LNA in* 0.13um *CMOS*, Proc. ISSCC'07, San Francisco, USA, Feb.2007, 2 pp.
11. N. Ahsan, C. Svensson and J. Dabrowski, *Highly Linear Wideband Low Power Current Mode LNA*, Proc. of ICSES, September 2008, Krakow, Poland, pp 73-76.
12. N. Ahsan, J. Dabrowski and A. Ouacha, *A Self-Tuning Technique for Optimization of Dual Band LNA*, Proc. of IEEE European Microwave Conference (EuMC), Oct. 2008, Amsterdam, the Netherlands, pp 178-181